CLAIMS

1. A memory system for a graphics processing system having a memory request bus to provide a direct memory access request to access memory, the direct memory access request including a memory address corresponding to a location in memory to be accessed, the memory system comprising:

a first addressable memory area defined by a first start address and a first size value to store graphics data;

a first memory controller coupled to the first addressable memory area and having a start address register and a memory size register for storing, respectively, the first start address and the first size value, the first memory controller coupled to the memory request bus to receive the direct memory access request and adapted to access the first addressable memory area in response to the memory address being located therein and to generate an indirect memory access request including the memory address otherwise;

a memory controller bus coupled to the first memory controller structured to transmit the indirect memory access request and to transmit graphics data;

a second addressable memory area defined by a second start address and a second size value to store graphics data; and

a second memory controller coupled to the second addressable memory area and having a start address register and a memory size register for storing respectively, the second start address and the second size value, the second memory controller further coupled to the memory controller bus to receive the indirect memory access request from the first memory controller and adapted to access the second addressable memory area in response to the memory address being located therein to service the direct memory access request received by the first memory controller.

2. The memory system of claim 1 wherein the second memory controller is further adapted to generate an indirect memory access request including the memory address in response to the memory address not being located within the second addressable memory area, the memory system, further comprising:

a third addressable memory area defined by a third start address and a third size value to store graphics data; and

a third memory controller coupled to the third addressable memory area and having a start address register and a memory size register for storing respectively, the third start address and the third size value, the third memory controller further coupled to the memory controller bus to receive the indirect memory access request from the second memory controller and adapted to access the third addressable memory area in response to the memory address being located therein to service the direct memory access request received by the first memory controller.

3. The memory system of claim 2 wherein the third memory controller is further adapted to generate an indirect memory access request including the memory address in response to the memory address not being located within the third addressable memory area, the memory system, further comprising:

a fourth addressable memory area defined by a fourth start address and a fourth size value to store graphics data; and

a fourth memory controller coupled to the fourth addressable memory area and having a start address register and a memory size register for storing respectively, the fourth start address and the fourth size value, the fourth memory controller further coupled to the memory controller bus to receive the indirect memory access request from the third memory controller and adapted to access the fourth addressable memory area in response to the memory address being located therein to service the direct memory access request received by the first memory controller.

4. The memory system of claim 1 wherein at least one of the first and second addressable memory areas comprises an embedded memory array fabricated with the first and second memory controller on a single semiconductor substrate.

5. The memory system of claim 1 wherein at least one of the first and second addressable memory areas comprises a plurality of memory arrays, each memory array contributing memory to the respective addressable memory area.

6. The memory system of claim 1 wherein at least one of the first and second addressable memory areas comprises a memory device having a memory array fabricated on a semiconductor substrate other than the one on which the first and second memory controllers are fabricated.

7. A graphics processing memory subsystem, comprising:

a first memory having first addressable memory area defined by first and second values;

a first memory controller coupled to the first memory and a first memory request bus to receive a memory access request to access a memory location, the first memory controller having first and second registers for storing the first and second values, respectively;

a memory controller bus coupled to the first memory controller;

a second memory having a second addressable memory area defined by third and fourth values; and

a second memory controller having first and second registers for storing the second the third and fourth values, respectively, the second memory controller coupled to the second memory and the memory controller bus to receive the memory access request if the memory location is not in the first addressable memory area.

8. The memory subsystem of claim 7, further comprising:

a third memory having third addressable memory area defined by fifth and sixth values; and

a third memory controller coupled to the third memory having first and second registers for storing the fifth and sixth values, respectively, the third memory controller coupled to the third memory and the memory controller bus to receive the memory access request if the memory location is not in the second addressable memory area.

9. The memory subsystem of claim 8, further comprising:

a fourth memory having fourth addressable memory area defined by seventh and eighth values; and

a fourth memory controller coupled to the fourth memory having first and second registers for storing the seventh and eighth values, respectively, the fourth memory controller coupled to the fourth memory and the memory controller bus to receive the memory access request if the memory location is not in the third addressable memory area.

10. The memory subsystem of claim 7 wherein at least one of the first and second memories comprises an embedded memory array fabricated with the first and second memory controllers on a single semiconductor substrate.

11. The memory subsystem of claim 7 wherein at least one of the first and second memories comprises a plurality of memory arrays, each memory array contributing memory to the first addressable memory area.

12. The memory subsystem of claim 7 wherein at least one of the first and second memories comprises at least one memory device fabricated on a semiconductor substrate different than the one on which the first and second memories are fabricated.

13. The memory subsystem of claim 7 wherein the first and third values comprise a start address value for the respective memory, and the second and fourth values comprise a memory size value for the respective memory.

14. A distributed memory controller memory system for a graphics processing system, comprising:

a first addressable memory area;

a second addressable memory area;

a first memory controller coupled to the first addressable memory area and having access to memory locations therein; and

a second memory controller coupled to the second addressable memory area and having access to memory locations therein, the second memory controller further coupled to the first memory controller through a first memory controller bus to receive memory access requests from the first memory controller requesting access to memory locations in the second addressable memory area.

15. The memory system of claim 14, further comprising:

a third addressable memory area; and

a third memory controller coupled to the third addressable memory area and having access to memory locations therein, the third memory controller further coupled to the second memory controller through a second memory controller bus to receive memory access requests from the second memory controller requesting access to memory locations in the third addressable memory area.

16. The memory system of claim 15, further comprising:

a fourth addressable memory area; and

a fourth memory controller coupled to the fourth addressable memory area and having access to memory locations therein, the fourth memory controller further coupled to the third memory controller through a third memory controller bus to receive memory access

requests from the third memory controller requesting access to memory locations in the fourth addressable memory area.

17. The memory system of claim 14 wherein the first memory controller includes first and second registers for storing first and second values, respectively, that define the first addressable memory area, and the second memory controller includes first and second registers for storing third and fourth values, respectively, that define the second addressable memory area.

18. The memory system of claim 17 wherein the first and second values are a start address and a memory size value for the first addressable memory area, respectively, and the third and fourth values are a start address and a memory size value for the second addressable memory area, respectively.

19. The memory system of claim 17 wherein the first and second values are a start address and an end address for the first addressable memory area, respectively, and the third and fourth values are a start address and an end address for the second addressable memory area, respectively.

20. The memory system of claim 14 wherein the first addressable memory area comprises a plurality of memory arrays, each memory array contributing a portion of memory to the first addressable memory area.

21. The memory system of claim 14 wherein the first addressable memory area comprises an embedded memory array and the first memory controller and the embedded memory array are fabricated on a single semiconductor substrate.

22. A distributed memory controller memory system for a graphics processing system, comprising:

a first memory and memory controller pair, the memory controller of the first pair having access to the memory of the first pair;

a second memory and memory controller pair, the memory controller of the second pair having access to the memory of the second pair; and

a memory controller bus coupling the memory controller of the first pair to the memory controller of the second pair,

wherein the memory controller of the first pair being structured to pass a memory access request it receives to the memory controller of the second pair over the memory controller bus in response to the memory controller of the first pair determining that the memory access request cannot be completed by it accessing the memory of the first pair.

23. The memory system of claim 22, further comprising a third memory and memory controller pair, the memory controller of the third pair having access to the memory of the third pair and being coupled to the memory controller bus to receive the memory access request from the memory controller of the second pair in response to the memory controller of the second pair determining that the memory access request cannot be completed by it accessing the memory of the second pair.

24. The memory system of claim 23, further comprising a fourth memory and memory controller pair, the memory controller of the fourth pair having access to the memory of the fourth pair and being coupled to the memory controller bus to receive the memory access request from the memory controller of the third pair in response to the memory controller of the third pair determining that the memory access request cannot be completed by it accessing the memory of the third pair.

25. A graphics processing system, comprising:

a bus interface for coupling to a system bus;

a graphics processor coupled to the bus interface to process graphics data;

address and data busses coupled to the graphics processor to transfer address and graphics data to and from the graphics processor;

display logic coupled to the data bus to drive a display;

a memory request bus coupled to the graphics processor to transfer memory access requests; and

a distributed memory controller memory subsystem coupled to the memory request bus to receive and service memory access requests, the memory subsystem comprising:

a first addressable memory area;

a second addressable memory area;

a first memory controller coupled to the memory request bus to receive memory access requests, the first memory controller further coupled to the first addressable memory area and having access to memory locations therein; and

a second memory controller coupled to the second addressable memory area and having access to memory locations therein, the second memory controller further coupled to the first memory controller through a first memory controller bus to receive memory access requests from the first memory controller requesting access to memory locations in the second addressable memory area.

26. The graphics processing system of claim 25 wherein the memory subsystem further comprises:

a third addressable memory area; and

a third memory controller coupled to the third addressable memory area and having access to memory locations therein, the third memory controller further coupled to the second memory controller through a second memory controller bus to receive memory access requests from the second memory controller requesting access to memory locations in the third addressable memory area.

27. The graphics processing system of claim 26 wherein the memory subsystem further comprises:

a fourth addressable memory area; and

a fourth memory controller coupled to the fourth addressable memory area and having access to memory locations therein, the fourth memory controller further coupled to the third memory controller through a third memory controller bus to receive memory access requests from the third memory controller requesting access to memory locations in the fourth addressable memory area.

28. The graphics processing system of claim 25 wherein the first memory controller of the memory subsystem includes first and second registers for storing first and second values, respectively, that define the first addressable memory area, and the second memory controller includes first and second registers for storing third and fourth values, respectively, that define the second addressable memory area.

29. The graphics processing system of claim 28 wherein the first and second values are a start address and a memory size value for the first addressable memory area, respectively, and the third and fourth values are a start address and a memory size value for the second addressable memory area, respectively.

30. The graphics processing system of claim 28 wherein the first and second values are a start address and an end address for the first addressable memory area, respectively, and the third and fourth values are a start address and an end address for the second addressable memory area, respectively.

31. The graphics processing system of claim 25 wherein the first addressable memory area of the memory subsystem comprises a plurality of memory arrays, each memory array contributing a portion of memory to the first addressable memory area.

32. The graphics processing system of claim 25 wherein the first addressable memory area of the memory subsystem comprises an embedded memory array and the first memory controller and the embedded memory array are fabricated on a single semiconductor substrate.

33. A computer system, comprising:

a system processor;

a system bus coupled to the system processor;

a system memory coupled to the system bus; and

a graphics processing system coupled to the system bus, the graphics processing system, comprising:

a bus interface for coupling to the system bus;

a graphics processor coupled to the bus interface to process graphics data;

address and data busses coupled to the graphics processor to transfer address and graphics data to and from the graphics processor;

display logic coupled to the data bus to drive a display;

a memory request bus coupled to the graphics processor to transfer memory access requests; and

a distributed memory controller memory subsystem coupled to the memory request bus to receive and service memory access requests, the memory subsystem comprising:

a first addressable memory area;

a second addressable memory area;

a first memory controller coupled to the memory request bus to receive memory access requests, the first memory controller further coupled to the first addressable memory area and having access to memory locations therein; and

a second memory controller coupled to the second addressable memory area and having access to memory locations therein, the second memory controller further coupled to the first memory controller through a first memory controller bus to receive

memory access requests from the first memory controller requesting access to memory locations in the second addressable memory area.

34. The computer system of claim 33 wherein the memory subsystem further comprises:

a third addressable memory area; and

a third memory controller coupled to the third addressable memory area and having access to memory locations therein, the third memory controller further coupled to the second memory controller through a second memory controller bus to receive memory access requests from the second memory controller requesting access to memory locations in the third addressable memory area.

35. The computer system of claim 34 wherein the memory subsystem further comprises:

a fourth addressable memory area; and

a fourth memory controller coupled to the fourth addressable memory area and having access to memory locations therein, the fourth memory controller further coupled to the third memory controller through a third memory controller bus to receive memory access requests from the third memory controller requesting access to memory locations in the fourth addressable memory area.

36. The computer system of claim 33 wherein the first memory controller of the memory subsystem includes first and second registers for storing first and second values, respectively, that define the first addressable memory area, and the second memory controller includes first and second registers for storing third and fourth values, respectively, that define the second addressable memory area.

37. The computer system of claim 36 wherein the first and second values are a start address and a memory size value for the first addressable memory area,

respectively, and the third and fourth values are a start address and a memory size value for the second addressable memory area, respectively.

38. The computer system of claim 36 wherein the first and second values are a start address and an end address for the first addressable memory area, respectively, and the third and fourth values are a start address and an end address for the second addressable memory area, respectively.

39. The computer system of claim 33 wherein the first addressable memory area of the memory subsystem comprises a plurality of memory arrays, each memory array contributing a portion of memory to the first addressable memory area.

40. The computer system of claim 33 wherein the first addressable memory area of the memory subsystem comprises an embedded memory array and the first memory controller and the embedded memory array are fabricated on a single semiconductor substrate.

41. The computer system of claim 33 wherein at least one of the first and second addressable memory areas of the memory subsystem is the system memory.

42. A method of accessing a memory location having a memory address in graphics processing system, comprising:

receiving at a first memory controller a memory access request to access the memory location;

determining whether the memory address of the memory location is within a first addressable memory area to which the first memory controller is coupled;

passing the memory access request to another memory controller to service the memory access request when the memory address is not within the addressable memory area which the first memory controller can access; and

accessing the memory location through a memory controller coupled to an addressable memory area containing the memory location.

43. The method of claim 42, further comprising:

if the memory access request is a read command, reading data from the memory location and returning the data to the first memory controller to complete the memory access request; and

if the memory access request is a write command, including write data with the memory access request and writing the write data to the memory location through the memory controller coupled to the addressable memory area containing the memory location.

44. The method of claim 42, further comprising storing in each memory controller first and second values defining the addressable memory area to which the respective memory controller is coupled.

45. The method of claim 44 wherein determining whether the memory address is within the first addressable memory area comprises comparing the memory address to the first and second values stored in the first memory controller.

46. The method of claim 44 wherein the first and second values are a start address and memory size value, respectively, for the respective addressable memory area.

47. The method of claim 44 wherein the first and second values are a start address and end address, respectively, for the respective addressable memory area.

48. In a graphics processing system, a method of accessing a memory location having a memory address, comprising:

receiving at a memory controller a memory access request to access the memory location;

comparing the memory address to first and second values that define an addressable memory area to which the memory controller can access;

forwarding the memory access request to another memory controller when the memory location is not located in the addressable memory area accessible to the receiving memory controller;

repeating the steps of receiving, comparing, and forwarding until a target memory controller identifies that the memory location is located within the addressable memory area to which the target memory controller is coupled; and

accessing the memory location through the target memory controller.

49. The method of claim 48, further comprising:

if the memory access request is a read command, reading through the target memory controller data from the memory location and returning the data to the memory controller that first received the memory access request; and

if the memory access request is a write command, including write data with the memory access request and writing the write data to the memory location through the target memory controller.

50. The method of claim 48, further comprising storing in each memory controller the first and second values for the addressable memory area to which the respective memory controller is coupled.

51. The method of claim 48 wherein the first and second values are a start address and memory size value, respectively, for the respective addressable memory area.

52. The method of claim 48 wherein the first and second values are a start address and end address, respectively, for the respective addressable memory area.